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EXAMINER	
VILLECCO, JOHN M	

ART UNIT	PAPER NUMBER
2612	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,679	BARNA ET AL.	
	Examiner	Art Unit	
	John M. Villecco	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16,18-20,22-24,26 and 29-32 is/are rejected.

7)☒ Claim(s) 17,21,25,27 and 28 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 March 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/6/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-14 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Regarding claim 1, applicant recites the limitation of "a column readout part which reads out said photosensing devices..." and "a gain stage, ... to increase a level of said column readout part". Clearly, the column readout part does not read out the photosensing devices. The charges captured by the photosensing devices are read out, not the actual photosensing devices. As for the gain stage, the level of the column readout part is not increased, the signal on the column readout part is increased. Since there is no mention in the specification of the column readout part reading out the photosensing device or of the gain stage increasing the level of the column readout part being increased, this wording is indefinite. For examination purposes it will be assumed that the column readout part reads out charges captured by the photosensing devices and the gain stage increases the level of the signal within the column readout part.

4. Claims 2-14 and 31 are rejected based upon their dependency to claim 1.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 15, 16, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Carroll et al. (U.S. Patent No. 6,160,578).**

7. Regarding ***claim 15***, Carroll discloses a high speed, increased bandwidth camera, which uses a plurality of A/D converters for processing pixels of different colors. More specifically, Carroll discloses a CCD (12), which would inherently include an array of photosensitive pixels producing output signals indicative of values of the pixels, first A/D converters (23' and 22''), which receive a first color (green), and second A/D converters (23'' and 22'), which receive a second color (red and blue). See Figure 3. Additionally, Carroll discloses that a programmable phase shifter (26) operates to provide staggered operation timings to each of the A/D converters. In column 10, line 39 to column 11, line 32, Carroll discloses that each of the A/D converters has it's own phase that is independently adjustable using the variable phase shift circuits (85-88). Therefore, since each of the A/D converters (22', 22'', 23', and 23'') are operated at independently different phases it follows that one of the A/D converters would inherently by started when a different one of the A/D converters is operating.

8. As for ***claim 16***, as mentioned above, A/D converters (23' and 22'') receive the green pixel signals and A/D converters (23'' and 22') receive the red and blue color pixels.

9. ***Claim 26*** is considered substantively equivalent to claim 15. Please see the discussion of claim 15 presented above.

10. Claims 18, 19, 22, 23, 29, 31, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999).

11. Regarding ***claim 18***, Pain discloses a CMOS image sensor designed to be ultra-low power, miniature, and integrated on a single chip. The CMOS includes a two-dimensional array of photosensitive pixels and timing and control logic. See Figure 1 and page 1, section 2. Furthermore, on page 4, section 4, titled "Chip Power Dissipation" discloses that the power is conserved by turning off the current flowing to circuit blocks that are not in used. The circuit blocks are interpreted to be the control parts.

12. As for ***claim 19***, Pain discloses the use of a voltage clamp that can be turned off when not in use. More specifically, Pain discloses in Figure 5 the use of voltage clamps to operate the A/D converters. As mentioned above, Pain discloses on page 4, section 4, titled "Chip Power Dissipation" discloses that the power is conserved by turning off the current flowing to circuit blocks that are not in used.

13. With regard to ***claim 22***, Pain discloses the use of DAC's to provide a controllable bias voltage. Furthermore, Pain discloses that since the DAC's are only used when the row is read out, the power used is small because they are only used for a small amount of time. See page 4, section 4, titled "Chip Power Dissipation".

14. Regarding ***claim 23***, as previously mentioned, Pain discloses the use of digital-to-analog converters (DAC's) to provide a bias current. See page 1, section 2 and page 3, column 2, 3rd paragraph.

15. As for ***claim 29***, Pain discloses the use of DAC's for generating bias for use in acquiring images. See page 1, section 2, titled "Imager Architecture and Operation". Furthermore, Pain discloses that low average power is achieved by selectively turning on and off the DAC's providing the bias currents. See page 4, section 4, titled "Chip Power Dissipation".

16. Regarding ***claim 32***, Pain discloses mirroring a bias current multiple times. See page 3, column 2, paragraph 3. Additionally, Pain discloses that circuit blocks with no activity are turned off when not in use. See page 4, section 4, titled "Chip Power Dissipation".

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. **Claims 1-4, 12, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999) in view of Shaw et al. (U.S. Patent No. 6,606,122)**.

19. Regarding ***claim 1***, Pain discloses a CMOS image sensor designed to be ultra-low power, miniature, and integrated on a single chip. The CMOS includes a two-dimensional array of photosensitive pixels and timing and control logic. See Figure 1 and page 1, section 2. Pain also discloses a column output part (circuits of Figure 2), and an output driving stage (ADC's). Additionally, Pain discloses that circuit blocks with no activity are turned off when not in use. See page 4, section 4, titled "Chip Power Dissipation".

Pain, however, fails to explicitly disclose the use of a gain stage to increase the level of the output part. Shaw, on the other hand, discloses that it is well known in the art to control the gain of a CMOS image sensor after reading out the pixel signals. More specifically, Shaw discloses in column 10, lines 34-65, that by changing the value VREF input to the A/D converters alters the dynamic range and thus the gain of the A/D converter. Therefore, Shaw discloses that it is well known in the art to include a gain stage in a CMOS image sensor to control the gain. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a gain stage in the image sensor of Pain so that an image's dynamic range and thus the gain of the image signal can be improved, thereby forming a higher quality image.

20. As for ***claim 2***, Figure 2 of Pain shows the column readout part operating in a charge mode.

21. With regard to ***claims 3 and 4***, Pain discloses the use of DAC's for generating bias for use in acquiring images. See page 1, section 2, titled "Imager Architecture and Operation". Furthermore, Pain discloses that low average power is achieved by selectively turning on and off the DAC's providing the bias currents. See page 4, section 4, titled "Chip Power Dissipation".

22. Regarding ***claim 12***, as mentioned above in the discussion of claim 1, the examiner is interpreting the output driving stage to be the A/D converters (ADC's).

23. With regard to ***claim 31***, Pain discloses the use of a plurality of different timing and control logic circuits, which inherently would have different outputs. See Figure 1. Additionally, Pain discloses that circuit blocks with no activity are turned off when not in use. See page 4, section 4, titled "Chip Power Dissipation".

24. **Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999) in view of Shaw et al. (U.S. Patent No. 6,606,122) and further in view of Guerrieri et al. (U.S. Patent No. 6,233,012)**.

25. As mentioned previously in the discussion of claim 1, both Pain and Shaw disclose all of the limitations of the parent claim. However, neither of the aforementioned references specifically discloses that the column readout part includes an element that minimizes a stray capacitance. Guerrieri, on the other hand, discloses that it is well known in the art to provide an element that minimizes stray capacitance in CMOS imagers. More specifically, in order to counter the metal line capacitance generated by the input line (212), a conductive shield line (218) is formed beneath the input line (212). See column 3, line 60 to column 4, line 30. Parasitic input capacitance slows the readout time and reduce or increases the amount of charge provided to the amplifier (col. 1, lines 18-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a structure to reduce the stray capacitance on the readout line of Pain so that readout time is not slowed.

26. **Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999) in view of Guerrieri et al. (U.S. Patent No. 6,233,012)**.

27. ***Claim 20*** is considered substantively similar to claim 5. Please see the discussion of claim 5 above.

28. **Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999)**.

29. Regarding ***claim 24***, as mentioned above in the discussion of claim 18, Pain discloses all of the limitations of the parent claim. However, Pain fails to explicitly disclose that the timing and control logic produces a converter reference voltage, a clamped voltage, and a common mode feedback voltage. However, Official Notice is taken as to the fact that it is well known in the art that CMOS image sensors include timing and control logic to generate converter reference voltages, clamped voltages, and common mode feedback voltages. These voltages are common voltages associated with the readout of the pixel signals. Furthermore, applicant seems to even admit that the generation of the voltages is typical on page 8, paragraph 0052 of the specification. Therefore, since there voltages are common in the operation of an APS CMOS image sensor, it would have been obvious to include these voltages in the APS imager of Pain.

30. **Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999) in view of Mangelsdorf (U.S. Patent No. 6,018,364).**

31. Regarding claim 30, as mentioned above in the discussion of claim 29, Pain discloses all of the limitations of the parent claim. However, Pain fails to explicitly disclose that the bias signals are clamped signals. Mangelsdorf, on the other hand, discloses that it is well known in the art to use a clamping circuit to provide a clamped bias signal. More specifically, as discussed in column 11, lines 21-34, Mangelsdorf discloses the use of a clamping circuit to apply a bias voltage to the correlated double sampling circuit. The clamping circuit is advantageous because the bias applied to the gain amplifiers can be optimized. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a clamped signal as the bias signal so the amplifiers are operated at their linear range.

Allowable Subject Matter

32. Claims 6-11, 13-14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

33. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 6, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the element that eliminates stray capacitance

includes a multiplexer formed in multiple stages, each stage having fewer than all of the full number of signals.

As for claim 7, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the gain stage includes isolation stages, which isolate an actual element carrying out the gain from input and output.

With regard to claim 8, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the gain stage includes an input unity gain buffer stage, an output unity gain buffer stage, and a gain stage coupled between the input and output unity gain buffers.

Regarding claim 13, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the A/D converter includes first and second A/D converters operating out of phase with one another.

34. Claims 17, 21, 25, 27, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35. The following is a statement of reasons for the indication of allowable subject matter:

As for claim 17, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the A/D converter are successive approximation A/D converters.

With regard to claim 21, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the element includes an optimized gain

element with first and second unity gain buffers, and a gain stage, said first and second unity gain buffers isolating the gain stage from the readout bus.

Regarding claim 25, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that each of the converter reference voltage, clamped voltage, and common mode feedback voltage are produced by separate, controllable sources, which are turned off when not in use.

As for claim 27, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the second timing is 50 percent of the way through a conversion cycle represented by the first timing.

With regard to claim 28, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the A/D converting comprises successive approximation A/D converting.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (571) 272-7319. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John M. Villecco
June 7, 2005

AUNG MOE
PRIMARY EXAMINER